Order Number: MCUK980901G8

Technical Guide

G520 Personal Cellular Telephone

Handheld Portable
EB-G520

Handsfree Car Mount Kit
EB-HF520Z

Dual Charger
EB-CR520

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CONTENTS

WARNINGS AND CAUTIONS

WARNING

The equipment described in this manual contains polarized capacitors utilising liquid electrolyte. These devices are entirely safe provided that neither a short-circuit nor a reverse polarity connection is made across the capacitor terminals. FAILURE TO OBSERVE THIS WARNING COULD RESULT IN DAMAGE TO THE EQUIPMENT OR, AT WORST, POSSIBLE INJURY TO PERSONNEL RESULTING FROM ELECTRIC SHOCK OR THE AFFECTED CAPACITOR EXPLODING. EXTREME CARE MUST BE EXERCISED AT ALL TIMES WHEN HANDLING THESE DEVICES.

Caution

The equipment described in this manual contains electrostatic sensitive devices (ESDs). Damage can occur to these devices if the appropriate handling procedure is not adhered to.

ESD Handling precautions

A working area where ESDs may be safely handled without undue risk of damage from electrostatic discharge, must be available. The area must be equipped as follows:

Working Surfaces - All working surfaces must have a dissipative bench mat, SAFE for use with live equipment, connected via a 1M2 resistor (usually built into the lead) to a common ground point.

Wrist Strap - A quick release skin contact device with a flexible cord, which has a built in safety resistor of between 5k2 and 1M2 shall be used. The flexible cord must be attached to a dissipative earth point.

Containers - All containers and storage must be of the conductive type.

Batteries

This equipment may contain an internal battery in addition to the external battery packs. These batteries are recyclable and should be disposed of in accordance with local legislation. They must not be incinerated, or disposed of as ordinary rubbish.

1 INTRODUCTION

1.1 Purpose of this Guide

This guide contains technical information for the Panasonic G520 personal cellular telephone system operating on the GSM network. Procedures for installing, operating and servicing (e.g. disassembly and testing) the telephone system are provided in the associated Service Manual.

1.2 Structure of the Guide

The guide is structured to provide service-engineering personnel with the following technical information on the GSM mobile telephone:

1. Interface details and relevant test points.
2. Functional description of each section of the mobile telephone.
3. Detailed description of each section of the mobile telephone.

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2 INTERFACES AND TEST POINTS

2.1 Introduction

This section provides details on connections between the RF and Baseband PCB and other interfaces on G520.

2.2 Interfaces

2.2.1 Baseband and RF

This details the 50-way connector between the RF and baseband PCB.

No.	Signal Name	RF <=> LOGIC	Function	Connection	Status
1	DI	==>	Downlink I signal		
2	DIX	==>	Downlink nI signal		
3	DQ	==>	Downlink Q signal		
4	DQX	==>	Downlink nQ signal		
5	GND	---			
6	BUZZ+	<==	Buzzer control signal	REGFB of Charge IC	
7	BUZZ-	<==	Buzzer control signal	Buzzer of Charge IC	
8	GND	---			
9	RF-ON	<==	RF common block power control signal	TSPACT(5) of GEMINI	H:On, L:Off
10	VBAT	---	Battery power supply	BAT_VOLT:ADIN1(10 BIT AD)	NiMH: 4.8 V
11	VBAT	---	Battery power supply	BAT_VOLT:ADIN1(10 BIT AD)	NiMH: 4.8 V
12	GND	---			
13	VDDR	<==	3.5 V DC/DC output power supply		3.44 V ± 5 %
14	VDDR	<==	3.5 V DC/DC output power supply		4.44 V ± 5 %
15	GND	---			
16	Tx_ON	<==	Transmitter block power control signal	TSPACT(10) of GEMINI	H:On, L:Off
17	nON_HOOK	==>	ON HOOK detection signal	IO(9) of GEMINI	not used
18	GND	---			
19	V_VIB	<==	Power supply for vibrator		
20	V_VIB	<==	Power supply for vibrator		
21	UI	==>	Uplink I signal		
22	UIX	==>	Uplink nI signal		
23	UQ	==>	Uplink Q signal		
24	UQX	<==	Uplink nQ signal		Li-ION: 7.2 V, NiMH: 4.8V
25	GND	<==			
26	3V CNT	<==			
27	SIM 5V	<==	5.0 V DC/DC output power supply for SIM		5.0 V ± 2.4 %
28	PA_ON	<==	PA power control signal	TSPACT(11) of GEMINI	L: RX & MON slot, H:TX slot
29	PA_RAMP	<==	RF output power control signal of PA	APC of VEGA (5 BIT DA)	64 step
30	RX_ON1	<==	Receiver block power control signal1	TSPACT(6) of GEMINI	H:On, L:Off
31	RX_ON2	<==	Receiver block power control signal2	TSPACT(7) of GEMINI	H:On, L:Off
32	LO2SEL	<==	2nd LO Frequency control signal	TSPACT(4) of GEMINI	H:Ignition On, L(Hi-Z):Ignition Off
33	OCE	<==	Output Cancel Enable signal	BCAL=TSPACT(1) of GEMINI	H: Enable
34	IFAGCEN	<==	IF AGC Enable signal for RX IC	TSPEN(4) of GEMINI	H: Enable, L: Disable
35	AFC	<==	TCVCXO Frequency Control signal	AFC of VEGA (13 BIT DA)	
36	PLL_CLK	<==	PLL & AGC serial interface signal: Clock	TSPCLK of GEMINI	
37	PLL_SD	<==	PLL & AGC serial interface signal: Data	TSPDO of GEMINI	
38	PLL_STRB	<==	PLL serial interface signal: Strobe	TSPACT(9) of GEMINI	H: Enable, L: Disable
39	GND	---			
40	13MHzCLK	==>	13 MHz Main Clock	MCLK (more than 0.5 V)	

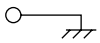
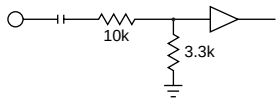
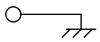
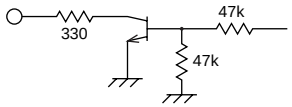
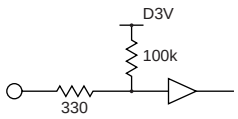
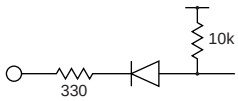
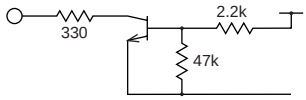
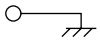
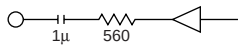
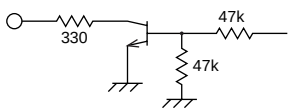
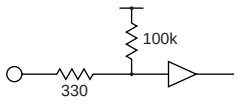
2.2.2 External Interface

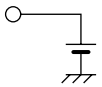
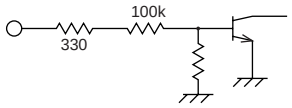
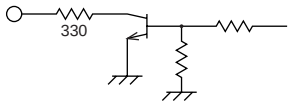
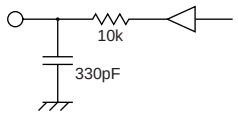
G520 has three external connectors:

1. a multi-way connector for use with a handsfree data;
2. additional contacts for charging the battery pack while in the desktop charger;
3. an RF connection for an external antenna and for test and measurement purposes.

All interfaces are electrically and mechanically compatible with G520.

Main Unit <==> External I/O

No.	Name	H/H <=> EXT	Function	H/H Circuit
1	GND	---	Power supply & digital signal ground	
2	TX-AUDIO	<==	Sending Audio	
3	AUDIO-GND	---	Ground for Audio	
4	nH/F-ON	==>	Handsfree path control signal (L: On, Hi-Z: Off)	
5	nADP-SENSE	<==	PCMCIA I/F Card discriminating signal (No connection: Open) (Data adaptor: GND) (RS232 direct cable: 33 kΩ pull-down) (SMS cable: 56 kΩ pull-down) (Headset adaptor: 82 kΩ pull-down)	
6	SERIAL-UP	<==	Upward serial (9600 bps: Test command) (9600 bps: SMS cable) (33.8 kbps Data adaptor I/F Card) (38.4 kbps: RS232 Direct cable)	
7	SERIAL-DOWN	==>	Downward serial (Baud rate is same as SERIAL-UP)	
8	EXT-PWR	<==	Power supply for battery charge	
9	GND	---	Power supply & digital signal ground	
10	RX-AUDIO	==>	Received Audio	
11	nRADIO-MUTE	---	RADIO MUTE Control (L: Radio Mute, Hi-Z: Radio Unmute)	
12	nH/F-SENSE	<==	H/F discriminating signal (L: existence, H: nothing)	

No.	Name	H/H <=> EXT	Function	H/H Circuit
13	VBAT	==>	Battery Output (4.5~8.4 V)	
14	IGNITION	<==	Can Ignition (L: Off, H: On)	
15	nLOGIC-PWR	==>	Peripheral power control (L: On, Hi-Z: Off)	
16	PA-ON	==>	PA control signal (L: Off, H 3 V: On)	
RF	TX-RX	<==>	Tx & Rx RF signal 50 Ω	

Charge Contacts

Pin	Signal	Description
20	EXT_PWR	Power for charging
21	GND	Ground

SIM Interface

Pin	Signal
1	GND
2	5 V
3	Not connected
4	Reset
5	Serial input/output
6	Clock
7	Not connected
8	Not connected

2.3 Test Points

2.3.1 Baseband

TP No.	Signal
402	TDI (U401 pin 88)
403	TDO (U401 pin 83)
404	nRESET
405	TCK (U401 pin 90)
406	TMS (U401 pin 91)
407	SIM_CLK_LO
412	TDI (U402 pin 63)
413	TDO (U402 pin 62)
414	TRST (U402 pin 24)
415	TCK (U402 pin 64)
416	TMS (U402 pin 61)
417	SSDR
418	SSDX
419	SSRST
420	SSCLK
421	TEST 1 (U402 pin 69)
422	TEST 2 (U402 pin 68)
423	TEST 3 (U402 pin 67)
425	CHARGE_LED
429	REC_P
430	REC_N
431	TX_AUDIO
432	RX_AUDIO
433	13MHzCLK
434	PA_ON
435	TX_ON
436	RX_ON2
437	RX_ON1
438	OCE
439	RF_ON
440	LO2SEL
441	nHF_TX_MUTE
442	VREF_OUT
443	SIM_CLK
444	SIM_IO
445	SIM_RST
446	BAT_TEMP
447	nADP_SENSE
448	nHF_SENSE
449	nON_HOOK
450	nLOGIC_POWER
451	IGNITION
452	SERIAL_UP
453	BATID
454	nHF_ON
455	SERIAL_DOWN
456	CHARGE_ON
457	KBC(0)
458	KBC(1)
459	KBC(2)
460	KBC(3)
461	KBC(4)
462	KBR(4)
463	KBR(3)
464	KBR(2)

TP No.	Signal
465	KBR(1)
466	KBR(0)
467	nPOWKEY
468	nRADIO_MUTE
469	AFC
485	VBAT
470	PARAMP
501	BUZON (U501 pin 19)
502	REGF8 (U501 pin 15)
503	nLVI
504	nRESET
505	BUZZER
506	PAGING_LED
486	EXT_PWR
508	VDD
510	VBAT
511	D5V
513	VDD
514	D3V
516	A3V

2.3.2 RF

TP No.	Signal
301	VDD
302	ULIP
303	ULIN
304	ULQN
305	ULQP
306	TX_ON
307	AFC
308	3VCONT
309	SIM5V
311	PA_ON
312	PA RAMP(APC)
313	RF_ON
314	LO2SEL
315	RX_ON1
316	PLL_SIRB
317	IFAGCEN
318	PLL_CLK
319	PLL_SD
320	BCAL(OCE)
321	DLIP
322	DLIN
323	DLQP
324	DLQN
325	RX_ON2
326	VBAT
310	GND

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3 RF OVERVIEW

3.1 Introduction

All the RF circuitry is contained on one PCB. The RF PCB has six layers made from FR4 material. Top and bottom layer tracks are gold-plated to prevent oxidisation and enable better soldering. The board thickness is 0.9 mm (± 0.1 mm).

The majority of the components are on one side of the PCB leaving as much as possible of the opposite side to be a complete ground plane; this is used to provide RF shielding.

The RF board is connected to the baseband digital board via a 60-way dual in-line connector.

The G520 RF PCB is a half-size board, i.e. half the dimensions of the handheld unit. In order to keep the PCB to these dimensions both sides of the board are populated with components. As there is no ground plane to improve shielding on one side of the RF, two chassis are needed, one either side. When the PCB is sandwiched between the two chassis it forms an effective shielded enclosure which prevents spurious emissions. The chassis have also been designed to provide smaller walled sections that are used to isolate sensitive areas such as the VCO from areas with high level RF signals such as the PA module output.

3.2 Functional Description

The major building blocks for the RF design are the transmit (Tx) and receive (Rx) ICs, RF-IF dual PLL and the antenna subsystem.

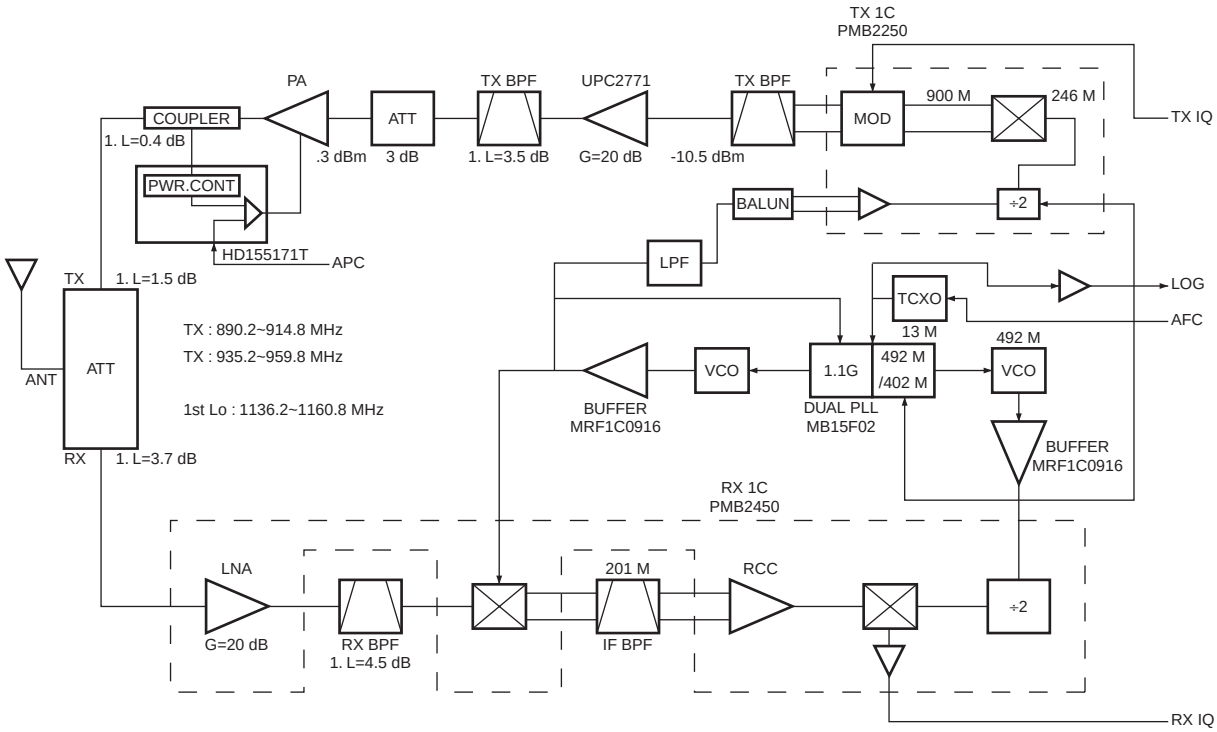


Figure:1 RF Block Diagram 520-0301

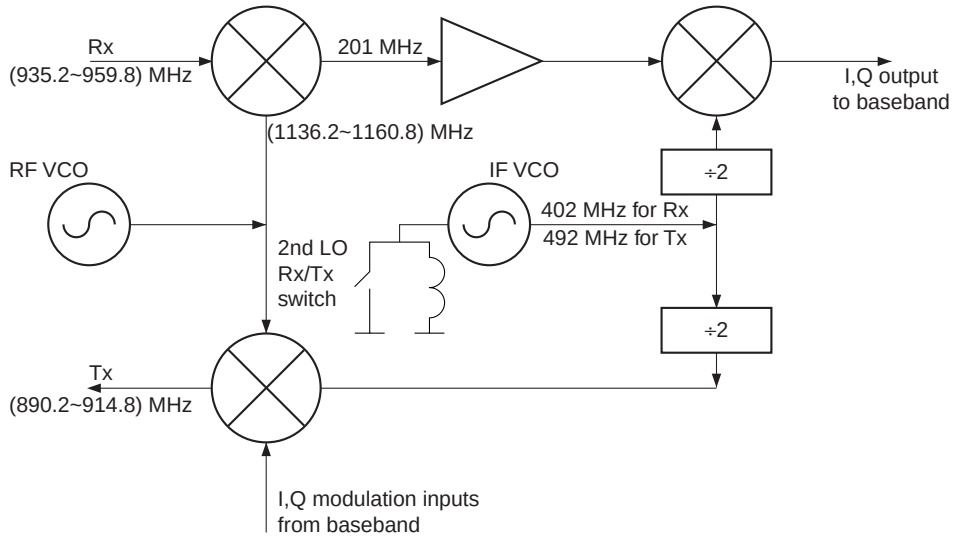


Figure:2 Frequency Plan 520-0302

3.2.1 Functional Description of the PLLs

The G520 design employs two fixed IF Los: 201 MHz for Rx and 246 MHz for Tx. They are generated at 402 MHz and 496 MHz using the IF part of the PLL (U307). The IF VCO used is a modular VCO between 402 MHz and 492 MHz by means of switching the frequency determined by the IFLOSEL control line.

The RF LO is generated by the PLL formed by the RF part of the PLL (U307) and an external modular VCO. The use of a modular VCO improves the design repeatability.

The 13 MHz clock generated by the TCXO is supplied through the TCXO buffer to eliminate logic noise. The TCXO buffer is active only during the period when the RF is turned on. When the RF is turned off in idle mode, the TCXO is switched off and another switching diode path is active to supply the clock to the logic. The technique decreases the idle current, hence increasing standby time.

3.2.2 Antenna

The antenna is a fixed helical type. A whip antenna may be connected to the RF path to provide better gain and minimise the head effects on the antenna.

A mechanical RF switch is used to route the RF signal from the external antenna for handsfree operation and test purposes.

3.2.3 Transmit and Receive

The transmit and receive paths of G520 are covered in their own specific chapters later in this manual.

4 TRANSMITTER

4.1 Introduction

This section provides a technical description of the transmitter circuit of the RF circuit. A circuit diagram of the whole system is provided in Section 8 of the Service Manual.

4.1.1 Uplink Frequencies

CHANNEL NUMBERS	UPLINK FREQUENCIES (MHz)				
1-5	890.200	890.400	890.600	890.800	891.000
6-10	891.200	891.400	891.600	891.800	892.000
11-15	892.200	892.400	892.600	892.800	893.000
16-20	893.200	893.400	893.600	893.800	894.000
21-25	894.200	894.400	894.600	894.800	895.000
26-30	895.200	895.400	895.600	895.800	896.000
31-35	896.200	896.400	896.600	896.800	897.000
36-40	897.200	897.400	897.600	897.800	898.000
41-45	898.200	898.400	898.600	898.800	899.000
46-50	899.200	899.400	899.600	899.800	900.000
51-55	900.200	900.400	900.600	900.800	901.000
56-60	901.200	901.400	901.600	901.800	902.000
61-65	902.200	902.400	902.600	902.800	903.000
66-70	903.200	903.400	903.600	903.800	904.000
71-75	904.200	904.400	904.600	904.800	905.000
76-80	905.200	905.400	905.600	905.800	906.000
81-85	906.200	906.400	906.600	906.800	907.000
86-90	907.200	907.400	907.600	907.800	908.000
91-95	908.200	908.400	908.600	908.800	909.000
96-100	909.200	909.400	909.600	909.800	910.000
101-105	910.200	910.400	910.600	910.800	911.000
106-110	911.200	911.400	911.600	911.800	912.000
111-115	912.200	912.400	912.600	912.800	913.000
116-120	913.200	913.400	913.600	913.800	914.000
121-124	914.200	914.400	914.600	914.800	

4.2 Functional Description

The main building block in the Tx line-up is the transmitter IC U102 that provides a Class 4 (2 Watts) transmitter.

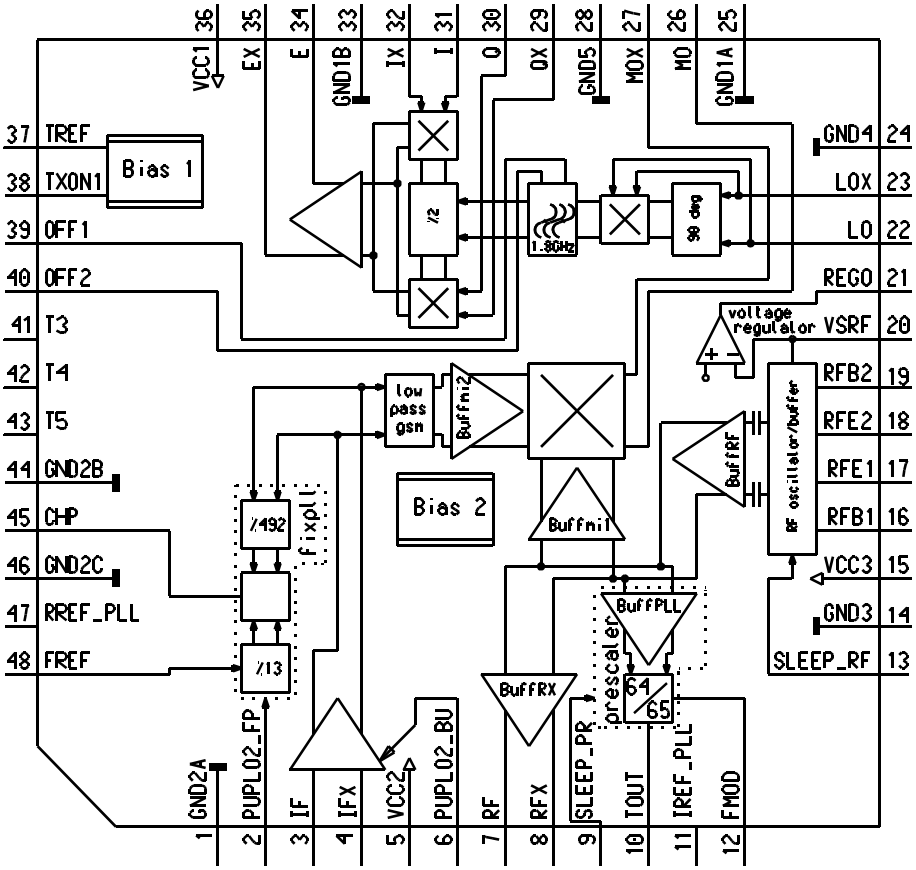


Figure:1 Transmitter IC U102 600-0401

The RF mixer is used to generate the GSM carrier, which is then modulated by the baseband I-Q signals in the quadrature modulator. The output from the quadrature modulator is buffered and is output differentially at about -8 dBm.

The RF LO is obtained from the same VCO that supplies the Rx LO, therefore the Tx IF frequency is 45 MHz greater than the Rx IF frequency. The IF LO is generated by the same discrete VCO as the Rx IF VCO offset by 90 MHz. The VCO frequency is divided by two by an on-chip divider to generate the required 246 MHz.

The output from Tx IC is filtered before and after the PA driver U103. The amount of filtering provided ensures that the Tx spurii and the Tx noise in the Rx band are within GSM limits with sufficient margins. Between FL101 and the PA there is a discrete attenuator to optimise the RF level into the PA and to provide some padding set to 2 dB.

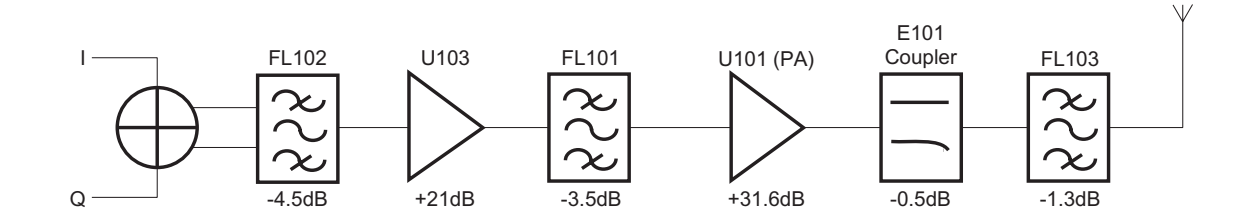
The PA amplifies the output from the PA driver to any required level up to PL5 (33 dBm) at the antenna. The power level can be controlled as required in Phase II GSM in 2 dB steps from 33 dBm to 5 dBm. To achieve the accuracy and time mask requirements for the output power, a closed loop power control design has been implemented. In this method, a portion of the output power (approx. -17 dB) is coupled into a detector. This sample is then compared with a ramp waveform whose rising and falling edges are precisely shaped to ensure that the frequency splash due to the fast turn on and off of the PA remains within specification. The level of the ramp waveform determines the output power level that needs to be transmitted.

The output from the PA is filtered through a discrete low-pass filter to ensure that there is sufficient margin in the rejection of the second and third Tx harmonics as the duplexer rejection is not sufficient.

For a typical output power of 33 dBm at the antenna, assuming a typical loss of 1.5 dB between the PA output and the antenna, the PA has an efficiency minimum of 40 %.

4.2.1 Signal Levels

The signal levels through the transmitter IC are given below.



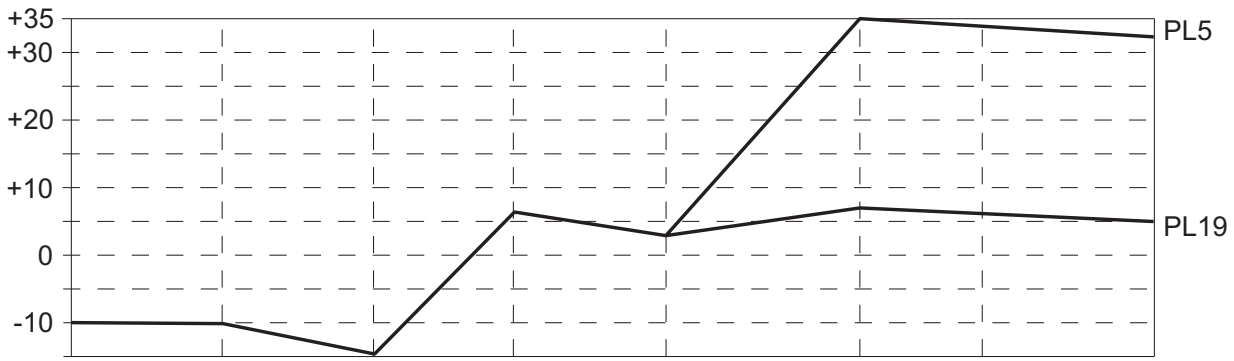


Figure:2 Typical Losses 520-0402

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5 RECEIVER

5.1 Introduction

This section provides a technical description of the receiver section of the RF circuit. A circuit diagram of the whole system is provided in Section 8 of the Service Manual (Order No. MCUK980901C8).

5.1.1 Downlink Frequencies

CHANNEL NUMBERS	DOWNLINK FREQUENCIES (MHz)				
1-5	935.200	935.400	935.600	935.800	936.000
6-10	936.200	936.400	936.600	936.800	937.000
11-15	937.200	937.400	937.600	937.800	938.000
16-20	938.200	938.400	938.600	938.800	939.000
21-25	939.200	939.400	939.600	939.800	940.000
26-30	940.200	940.400	940.600	940.800	941.000
31-35	941.200	941.400	941.600	941.800	942.000
36-40	942.200	942.400	942.600	942.800	943.000
41-45	943.200	943.400	943.600	943.800	944.000
46-50	944.200	944.400	944.600	944.800	945.000
51-55	945.200	945.400	945.600	945.800	946.000
56-60	946.200	946.400	946.600	946.800	947.000
61-65	947.200	947.400	947.600	947.800	948.000
66-70	948.200	948.400	948.600	948.800	949.000
71-75	949.200	949.400	949.600	949.800	950.000
76-80	950.200	950.400	950.600	950.800	951.000
81-85	951.200	951.400	951.600	951.800	952.000
86-90	952.200	952.400	952.600	952.800	953.000
91-95	953.200	953.400	953.600	953.800	954.000
96-100	954.200	954.400	954.600	954.800	955.000
101-105	955.200	955.400	955.600	955.800	956.000
106-110	956.200	956.400	956.600	956.800	957.000
111-115	957.200	957.400	957.600	957.800	958.000
116-120	958.200	958.400	958.600	958.800	959.000
121-124	959.200	959.400	959.600	959.800	

5.2 Functional Description

The main building block for the receiver is the IC U201. The receiver is a double superhet type with the first IF at 201 MHz; this is then converted down to zero IF.

The Rx IC contains the following stages:

1. LNA.
2. RF mixer.
3. Gain controlled 5-stage IF amplifier.
4. I,Q quadrature down converter.
5. Baseband Op Amps for further amplification and some filtering of the baseband I,Q signals.

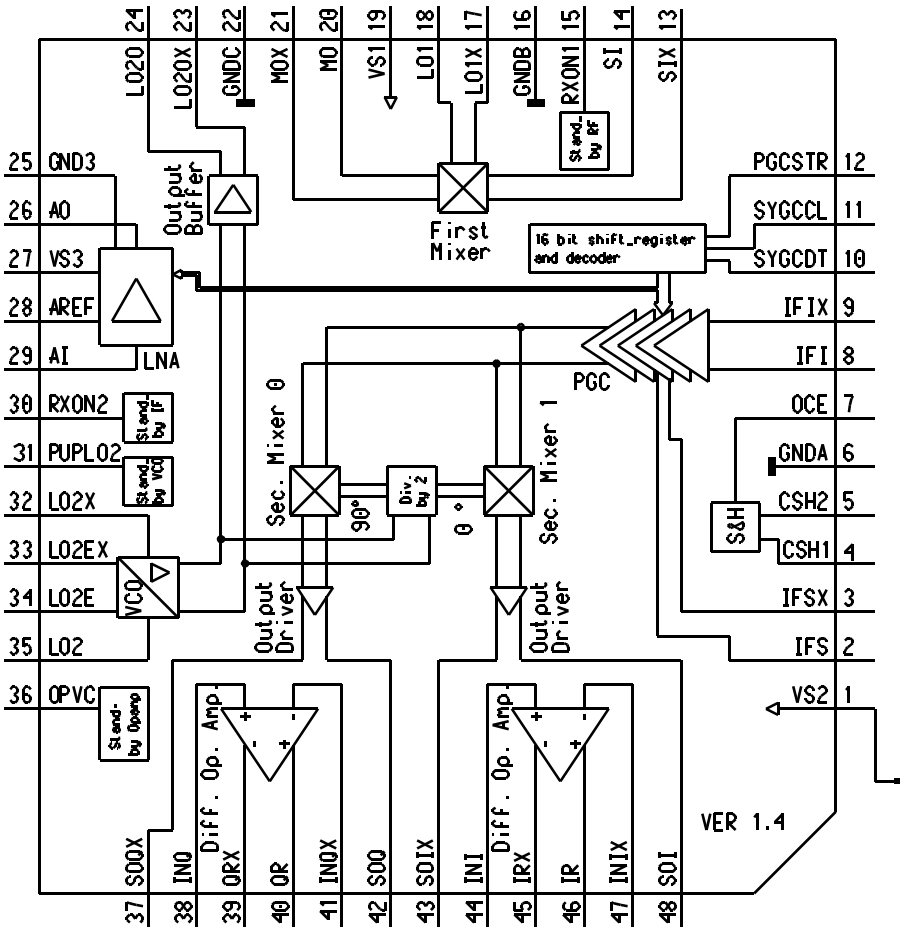

Figure:1 Receiver IC U201 600-0501

RF input to the receiver is either via the antenna or via the I/O connector for test purposes and handsfree operation. The input signal from the antenna or the I/O connector is fed into the LNA through the ANT - Rx path of the ceramic duplexer (FL103). The duplexer provides a filter function for the Tx signals between its Tx and ANT ports and an additional notch in the Rx band to minimise the Tx noise within the Rx band. The response between the ANT and Rx ports is a bandpass filter response providing the roofing filter function for the Rx front end.

The LNA gain can be controlled via a three-wire bus between a typical value of 20 dB and approximately -3 dB. The LNA gain reduction is required for operation under strong signal conditions where input power levels are greater than about -30 dBm.

The output from the LNA goes through a differential BP SAW filter and is differentially fed into the 1st down-converter mixer. The LO for the mixer is generated by a PLL (U307) employing a modular VCO (U303). The output from the VCO is buffered by an RF MMIC amplifier (U304). The LO frequency range is 1136.2 to 1160.8 MHz.

The IF output at 201 MHz from the mixer is filtered by the differential IF SAW filter (FL202) before it is fed into the gain-controlled IF amplifiers. The use of differential filters eliminates the need for baluns and provides some space advantage.

The IF amplifier is a five stage cascaded section. The gain is controllable by a three-wire bus from -10 to +70 dB in 2 dB steps. This function is used for AGC purposes.

The output from IF amplifiers is fed into two quadrature mixers where it is converted down to its baseband. The IF LO is generated at 402 MHz by an external discrete VCO. An on-chip divider on the Rx IC divides this by two and also produces two outputs in quadrature to generate the baseband I and Q signals. The outputs from the mixers are connected to external pins through a pair of buffers. Two on-chip Op Amps are used to amplify the AC signal from the mixers to meet the overall signal budget requirements.

The DC level at the output of the Op Amps is 0.95 V and a resistive DC adder is used to increase this DC level to 1.425 V as required by the baseband IC VEGA (see Section 8).

The coupling between RF output and the baseband input has been designed as a DC coupling in order to minimise the turn-on time of the Rx IC for the purpose of current optimisation.

5.2.1 Signal Levels

The signal levels through the receiver IC are given below.

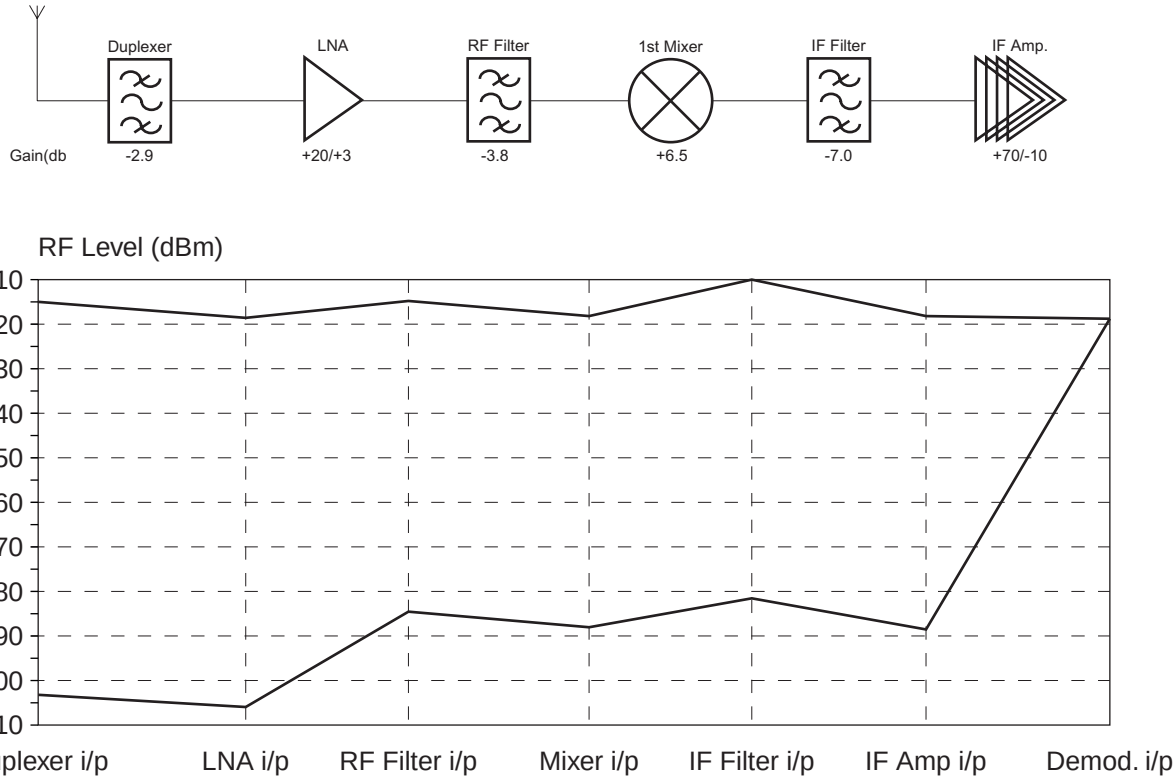

Figure:2 Nominal and Worst Case Signal Levels 520-0502

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6 BASEBAND OVERVIEW

6.1 Introduction

All Baseband circuitry is contained on one PCB. The Baseband PCB has six layers made from FR4 material. Top and bottom layers are gold-plated to prevent oxidisation and enable better soldering. The board thickness is 1.0 mm (+0.0, -0.1 mm).

The Baseband board is connected to the RF board via a 50 way dual in line connector.

A metallised plastic chassis is used to separate the Baseband and the RF PCBs. The continuous chassis design is important for EMC purposes. When the chassis is sandwiched between the Baseband and the RF PCBs the ground plane of the RF board together with the chassis forms an effective shielded enclosure, which prevents spurious emissions.

6.2 Functional Description

The G520 baseband is based around a 2 chip GSM chipset. One chip (GEMINI) carries out signal processing with DSP and CPU, and the other chip (VEGA) contains the analogue interface chip. The highly integrated nature of these components means each contain a large number of functions.

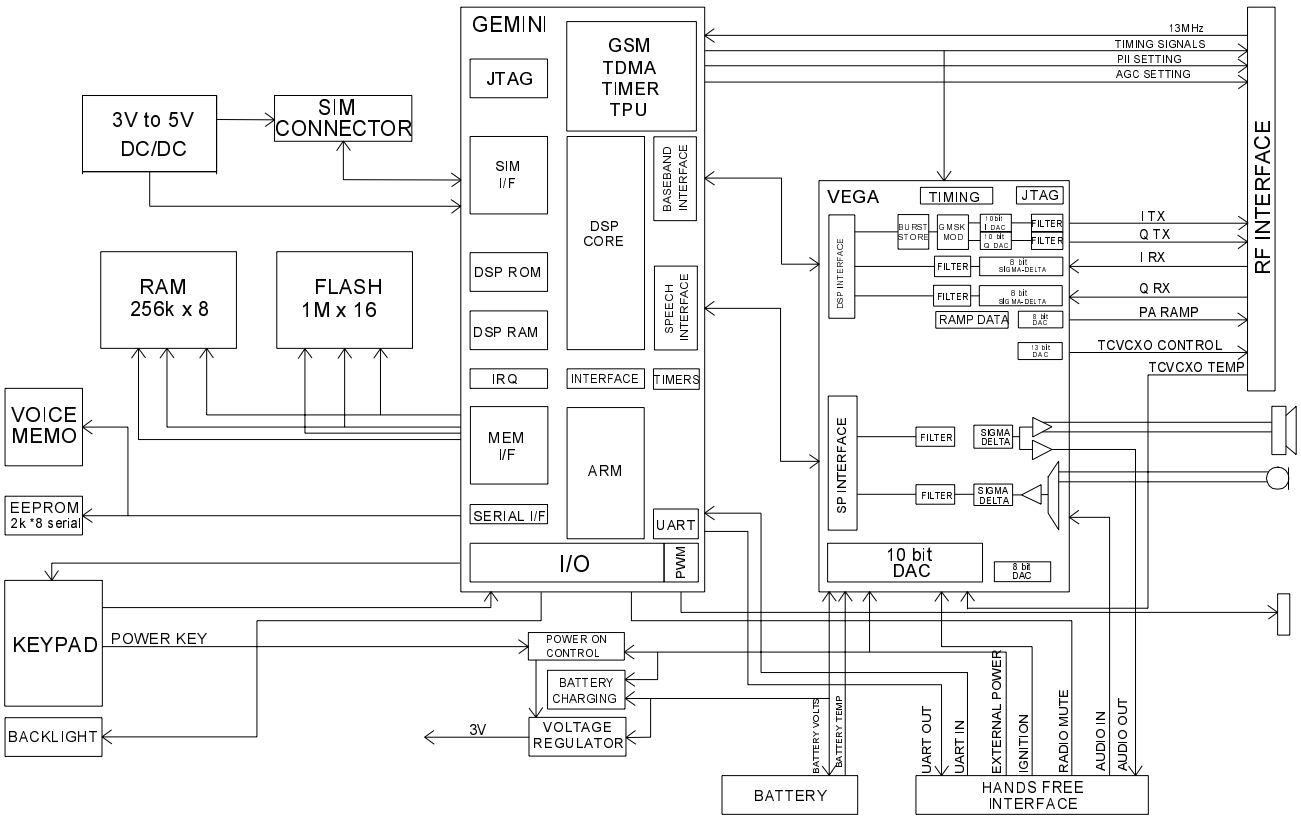

Figure:1 Baseband Block Diagram 600-0601

6.2.1 Keypad

The Keypad has a 5 x 5 matrix allowing 25 keys to be scanned on a key being pressed, a keypad interrupt is generated. To find which key is pressed the software must assert each column in turn and read which row is active.

To eliminate key bounce, the key press must then be confirmed twice at about 20 ms intervals. Because the End Key is also used to power on the phone it is allocated a complete row of the keyboard scan.

The Keyboard scanning is software controlled. Key pressed is indicated by an interrupt, but key release is controlled by software.

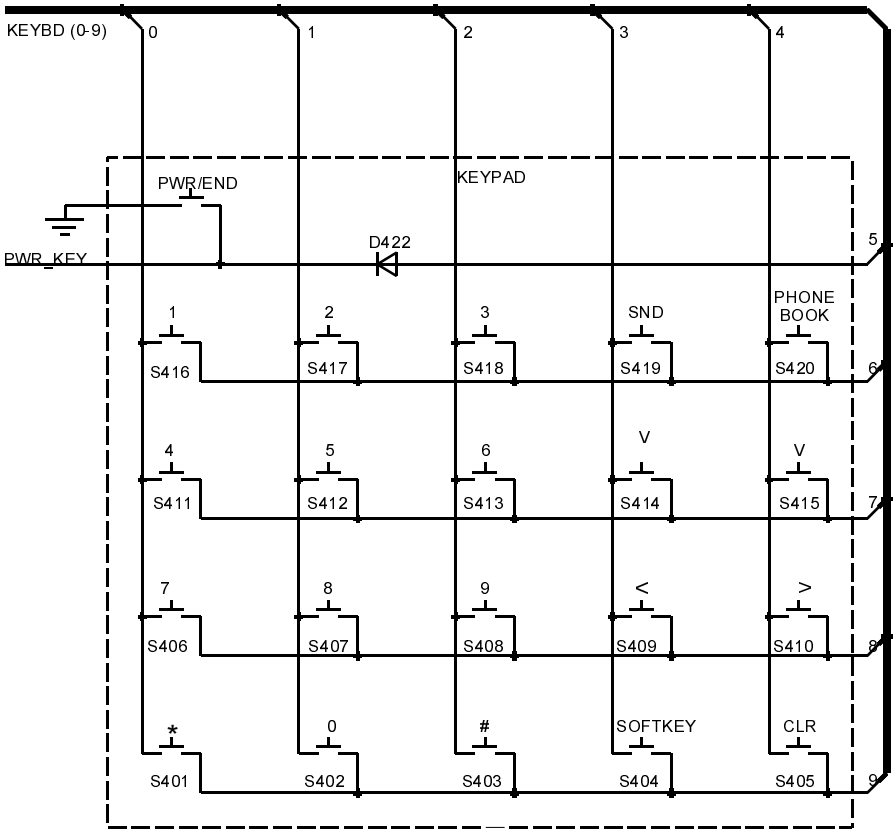

Figure:2 Keypad Matrix 600-0602

6.2.2 Subscriber Identity Module (SIM)

The SIM interface is designed for 5 V SIMs, this requires the addition of a 5 V step up regulator to provide the Interface requirements for a 5 V SIM.

The SIM outputs are open drain, and the inputs are 5 V tolerant. To achieve the required rise time on the clock line a transistor must be used to pull the clock high.

6.2.3 Time Processing Unit (TPU)

The TPU provides the GSM TDMA timing requirements for the system, external timing signals are provided by an area of Microcode within the GEMINI chip.

GEMINI Pin	Description
65	VEGA BENA
66	VEGA BCAL
67	VEGA BULON
68	VEGA BDLON
69	RF signal IFLOSEL
70	RF signal LO_EN
118	RF signal RXON1
119	RF signal RXON2
58	Used as nTSPEN (0) (VEGA SELECT)
59	Used as nTSPEN (4) (PLL_STRB)
60	RF signal TXON
61	RF signal PAON
62	Used as TSPEN (4) (IFAGCEN)

6.2.4 CPU Memory

The memory requirements for G520 are:

1. 16 Mbit 3 V FLASH organised as 1M * 16;
2. 2 Mbit 3 V RAM organised as 256k * 8;
3. 16 kbit 3 V Serial EEPROM as 2k * 8.

6.2.5 LCD

The LCD assembly is a subassembly comprising of LCD glass and driver chip on a flexible PCB with connection to the Logic PCB.

A 96 x 58 pixel graphical display is used to give maximum information. It can also display Chinese characters and large numbers. For example, 12 x 12 line or 16 x 3 line, both with 2 lines of icons.

A Sharp LH155B display driver is used.

6.2.6 Microphone

To provide improved speech pick-up, noise immunity and reduced echo the microphone is a noise canceling type (the noise canceling microphone requires a FLIP for acceptable frequency response). GSM requires that the sending audio frequency response must fit within the mask shown below.

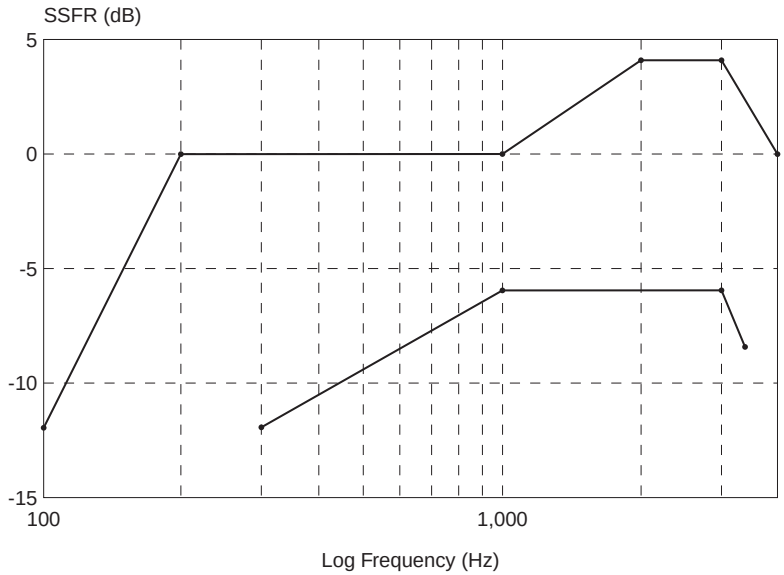

Figure:3 GSM Transmit Audio frequency response mask 520-0603

6.2.7 Speaker

VEGA runs from a 2.7 V supply, so a high impedance ceramic speaker will not satisfy user requirements for volume. A lower impedance (dynamic) type speaker must be used. GSM requires that the receive audio frequency response must fit within the mask shown below.

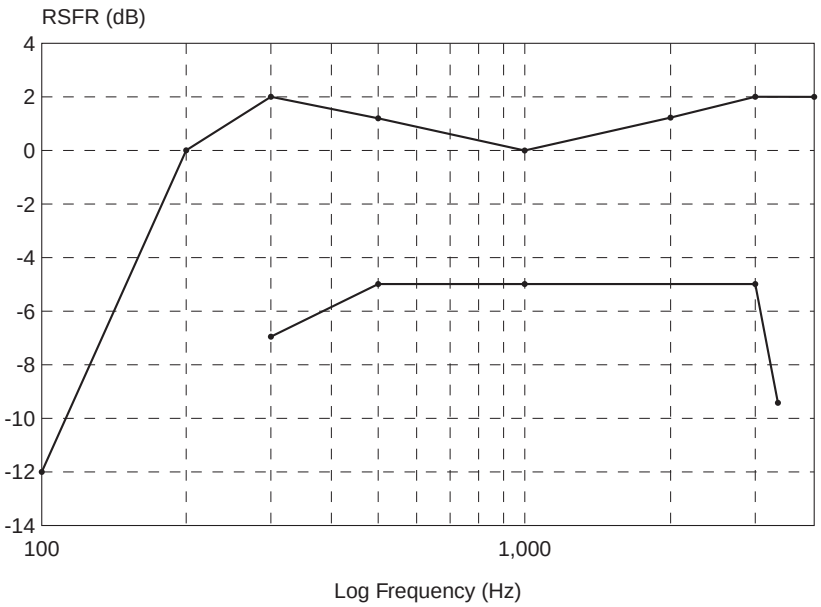

Figure:4 Audio frequency response 520-0604

6.2.8 Buzzer

The volume level of the buzzer is defined by the 6 bit PWM register setting in GEMINI I/O. The buzzer tone is then superimposed on this level using software.

Timer 1 in GEMINI is used to time the period between switching the buzzer on and off to make the tone. For more complex buzzer ringing tones, the buzzer volume level can also be altered after each time-out of timer 1.

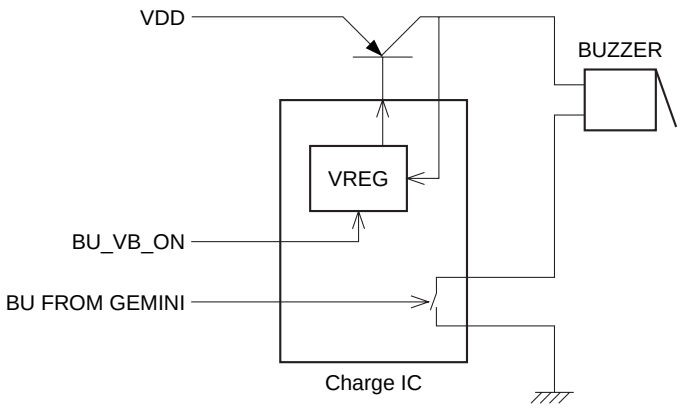

Figure:5 Buzzer Control Circuit 520-0605

7 GEMINI

7.1 Introduction

Gemini contains the DSP, CPU and GSM timing functions and many peripheral functions. The software for the DSP is contained in masked ROM.

7.2 Functional Description

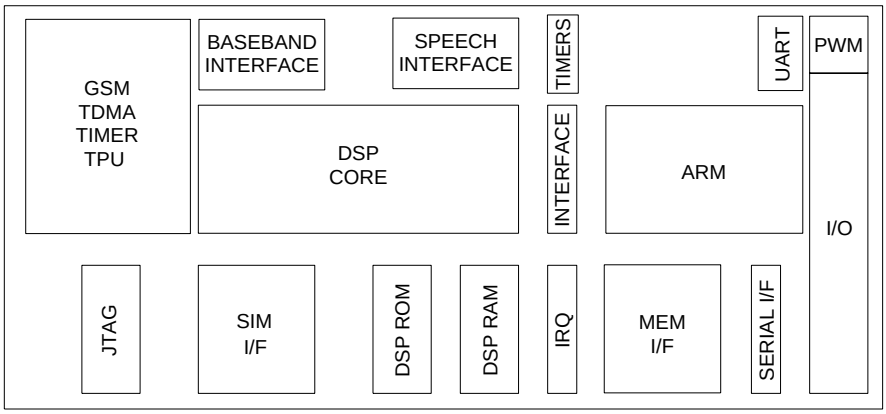

Figure:1 GEMINI Block Diagram 600-0701

7.2.1 Digital Signal Processor

The Digital Signal Processor (DSP) core is compatible with the Texas Instruments TMS350C5xx family of DSPs. Included in the DSP core is an interface to the CPU by a shared memory interface.

The DSP memory is also located within GEMINI. The ROM code size is determined by the size of the software.

7.2.2 CPU

The CPU is a 32 bit RISC CPU with 16 bit instruction set. The CPU is designed to access 32 bit memory and peripherals; a further module within the GEMINI chip allows access to 8 or 16 bit memory.

Memory Access Times		
Clock Speed	**Memory Access Time**	**Additional Access time per wait state**
19.5 MHz	41 ns	51 ns
13 MHz	67 ns	77 ns
9.75 MHz	91 ns	102 ns
6.5 MHz	144 ns	154 ns
4.875 MHz	194 ns	204 ns
3.75 MHz	298 ns	308 ns

For 120 ns access FLASH and RAM a 6.5 MHz clock gives 1 wait state access to both devices.

7.2.3 Memory Interface

The memory interface allows the 32 bit CPU to access 16 and 8 bit devices, and allows the addition of wait states to memory access. The memory interface allows between 0 and 7 wait states to be added. The ROM area is hardware write protected, a FLASH write enable bit in the ROM wait state configuration register can be used to enable write access the ROM area.

CPU Memory MAP				
Device Name	**Start address**	**Size**	**Use**	**Bus width**
ROM	0000:0000	2M	FLASH 1 Mbytes	16 bits
RAM	0020:0000	2M	RAM 256 kbytes	8 bits
BUS CNTRL	0040:0000	1M	wait state registers	16 bits
API RAM	0050:0000	8k	CPU/DSP shared ram	16 bits
TPU RAM	0050:0000	8k	GSM timer Microcode RAM	16 bits
APIC	0050:4000	1k	CPU/DSP interface controller	16 bits
SIM	0050:4800	1k	SIM interface	16 bits
TSP	0050:4C00	1k	Timed Serial port	16 bits
INTH	0050:5000	1k	Interrupt controller	16 bits
TPU REG	0050:5400	1k	GSM timer registers	16 bits
CLKM	0050:5800	1k	Clock control module	16 bits
TIMER	0050:5C00	1k	software timers	16 bit
APIF	0050:6000	1k	ARM peripheral interface	16 bit
UWIRE	0050:6400	1k	Synchronous Serial port	16 bit
ARMIO	0050:6800	1k	Keypad, buzzer, LCD & I/O	8 bit
8251	0050:6C00	1k	UART	8 bit
CS2	0060:0000	2M	LCD driver	8 bit
nCS0	0080:0000	2M	Extended I/O	8 bit
nCS1	00A0:0000	2M	not used	-

7.2.4 Interrupt Handler

The ARM CPU has 2 interrupts, FIQ is a Fast non-maskable interrupt and IRQ is a standard maskable interrupt.

Gemini has 11 interrupt sources. The Interrupt handler assigns priorities to these interrupts and routes them to either the FIQ or IRQ inputs of the ARM CPU. Additionally, the interrupt handler controls waking up of the CPU on receiving an unmasked interrupt, if the CPU is in sleep mode.

For G520 the FIQ interrupt is reserved for the power supply fail priority interrupt.

Interrupt Level Assignments		
Interrupt source	**Description**	**Interrupt detection**
IRQ_TIM1	Buzzer timer	Edge sensitive
IRQ_TIM2	operating system timer	Edge sensitive
IRQ_API	DSP Interface interrupt	Edge sensitive
IRQ_EXT	Power supply fail interrupt	Level sensitive
IRQ_USART	UART Interrupt	Level sensitive
IRQ_ARMIO	Keypad Interrupt	Low for 1 clk period
IRQ_FRAME	Frame Interrupt	Edge sensitive
IRQ_PAGE	Page Interrupt	Edge sensitive
IRQ_TIM_GSM		Edge sensitive
IRQ_TSP	Timed serial port Interrupt	Edge sensitive
IRQ_SIM	SIM Interrupt	Level sensitive
IRQ_F_USART	Fast interrupt from USART	Level sensitive
IRQ_RSS	Radio subsystem interrupt	Edge sensitive

7.2.5 General Purpose I/O

The general purpose I/O includes keypad scanning, 2 PWM ports and 16 I/O general purpose I/O lines. The general purpose I/O lines are multiplexed onto other functions, if I/O is selected the other function is unavailable.

I/O Pin Assignments			
Signal	**Gemini Pin**	**Use**	**Signal**
I/O (0) /nLCDCS	117	nLCDCS	
I/O (1) /RXE	116	STAY_ALIVE	H = PSU kept on L = PSU off
I/O (2) /TXE	115	VEGA_PWRDWN	L = Vega powered-up H = Vega powered-down
I/O (3) /DTR	114	HF_ON_	L = Hands free Off H = Hands free On
I/O (4) /DSR	110	RADIO_MUTE	L = Radio Mute Off H = Radio Mute On
I/O (5) /EXTINT	109	EXTINT	
I/O (6) / nRESETOUT	106	PA_LOW	H = Low RF Power level L = High RF power level
I/O (7) / SIM_RnW	105	CHARGE_LED	L = Charging LED off H = Charging LED on
I/O (8) /SIMPWCTRL	104	SIM_PWR	
I/O (9) /SIM_CD	95	nON_HOOK	H = Off _hook L = On hook
I/O (10) /LT	134	LT (LED output)	
I/O (11) /CLK32	73	nHF_DETECT	H = No Hands Free L = Hands Free connected
I/O (12) /TSPACT(0)	65	TSPACT (0)	
I/O (13) /nPWRCS	56	nPWRCS	
I/O (14) /nCS1	50	PAGING_LED	L = Paging LED off H = Paging LED On
I/O (15) /nCS0	49	CHARGE_ON	H = Charger On L = Charger Off
2 outputs have 6 bit PWM capability clocked at 2 MHz:			
LT	134	LED backlight	
BU	120	Buzzer	

Tones are generated by using timer 1 to switch the buzzer PWM on and off at a the frequency of timer 1. By altering the value of timer 1 ringing tunes can be played.

During hands free operation the ringing tone is derived from the DSP using its tone generator.

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8 VEGA

8.1 Introduction

VEGA contains the interface circuits to the Audio, RF and auxiliary analogue functions for the baseband circuit.

8.2 Functional Description

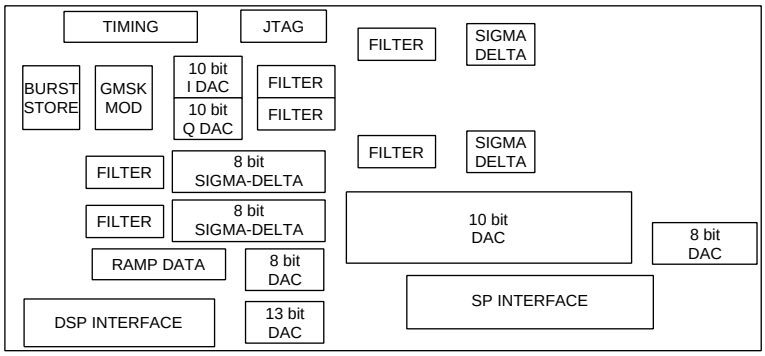

Figure:1 VEGA Block Diagram 600-0801

8.2.1 Uplink I and Q

VEGA performs GMSK modulation on .dData samples received from GEMINI at 270 kbits per second.

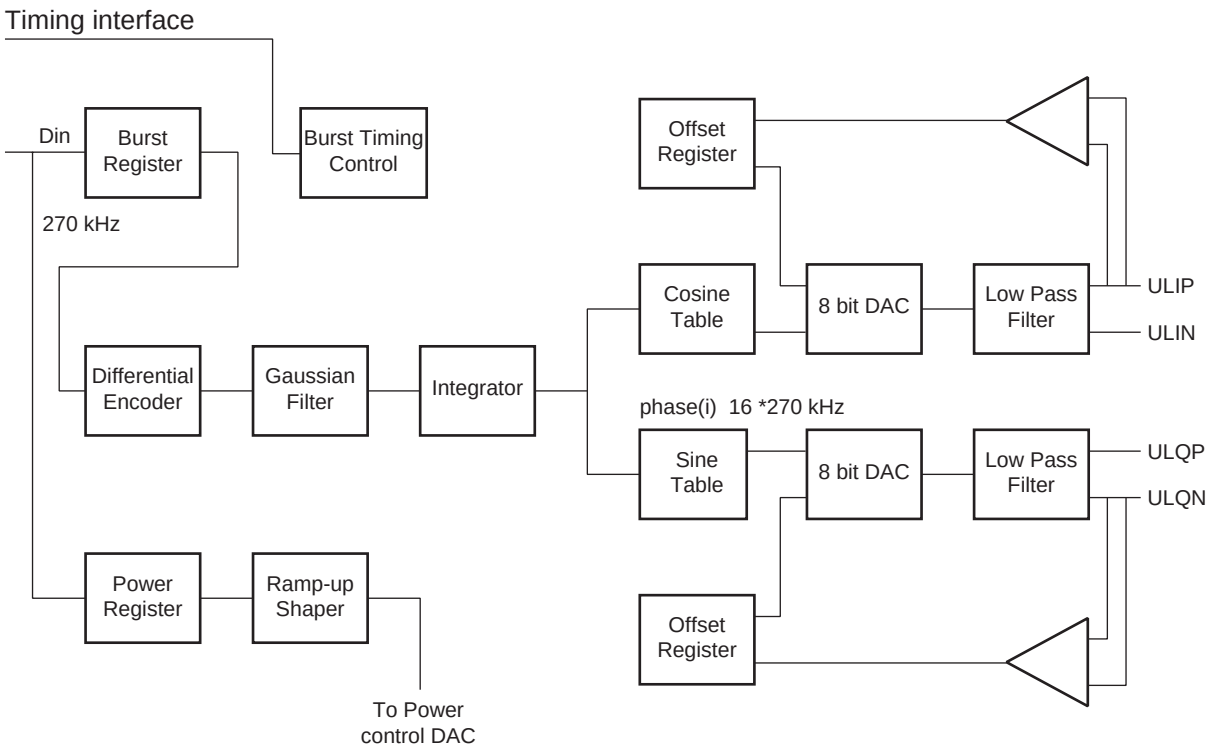

Figure:2 Functional structure of the baseband uplink path 600-0802

8.2.2 Downlink I and Q

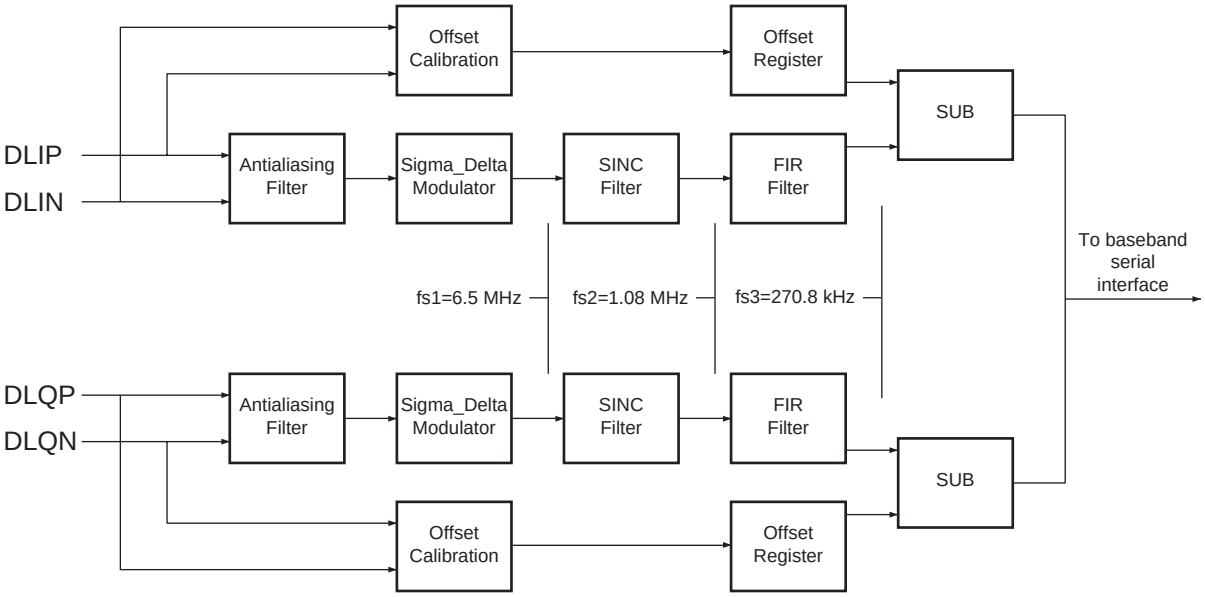

Figure:3 Functional structure of the baseband downlink path 600-0803

8.2.3 Power Amplifier Ramp

The PA Ramp is formed by 2 D/As. The first, a 5 bit D/A, defines the ramp shape; the second, an 8 bit D/A, defines the maximum level.

The ramp shape is defined by 64 steps. The shape can be defined differently for rising and falling ramps. Typically a raised cosine shape will be used as a starting basis of the ramp shape.

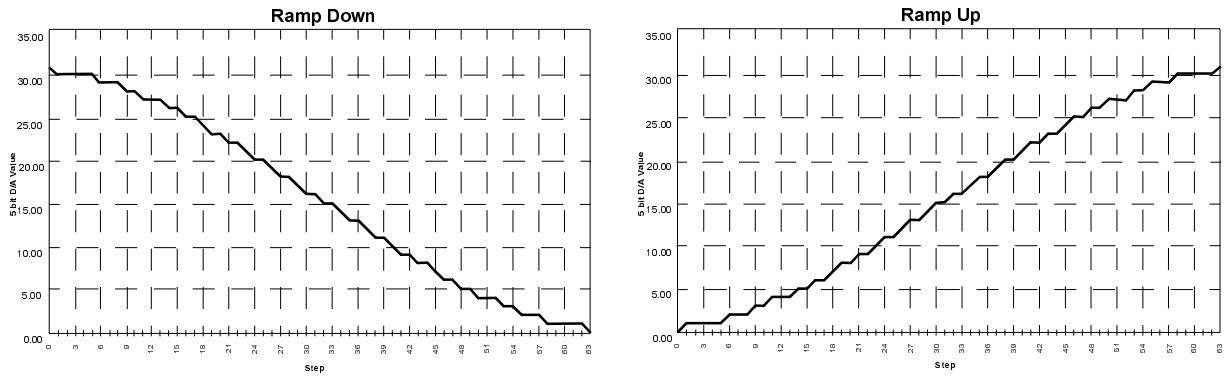

Figure:4 Example for the PA ramp 600-0804

The raised cosine shape will be modified to compensate for RF circuit characteristics.

The ramp time is selectable between each step being 1/16 of a bit and each step being 1/8 of a bit giving a maximum ramp time of either 14.77 µs or 29.53 µs.

An 8 bit value is used to program the ramp output level.

8.2.4 AFC Control

The 13 MHz system clock frequency is controlled by a 13 bit sigma-delta D/A in the VEGA chip

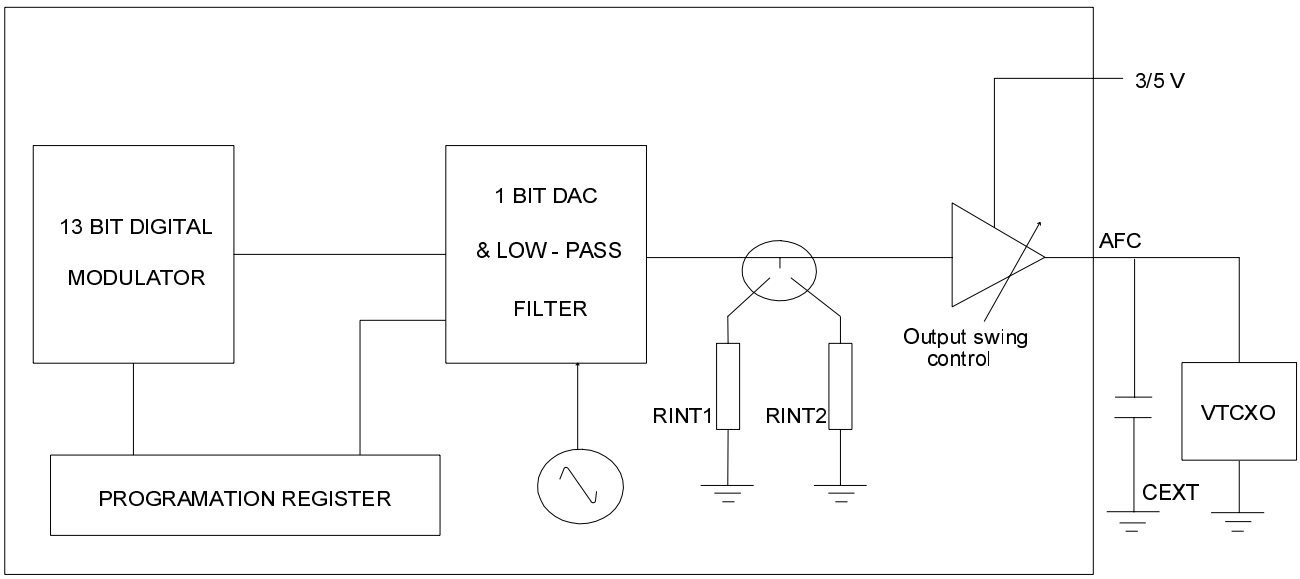

Figure:5 AFC block diagram 600-0805

8.2.5 Audio

VEGA provides the analogue interface for the digital audio samples processed by the DSP in GEMINI.

Voice Uplink Path

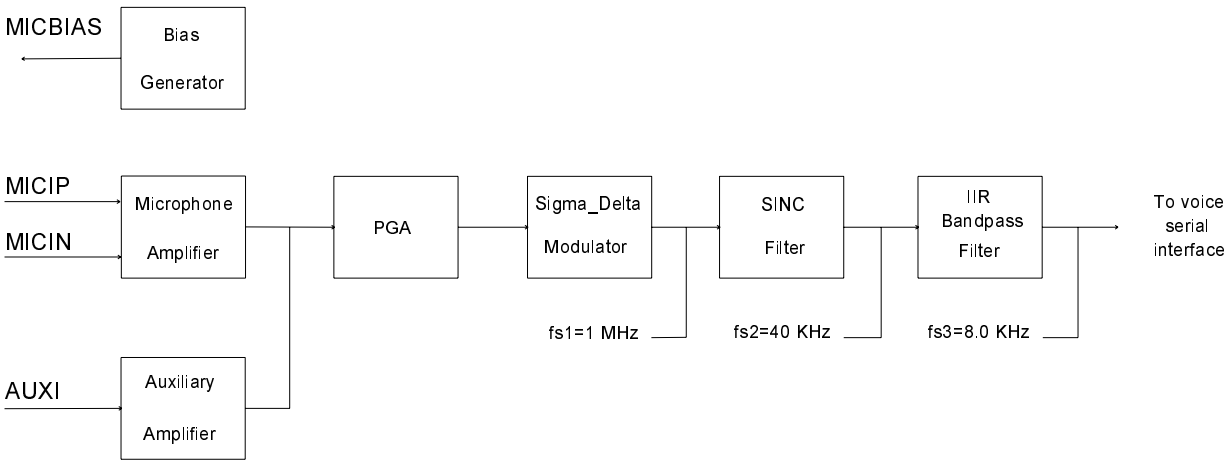

Figure:6 Voice ADC block diagram 600-0806

Voice Downlink Path

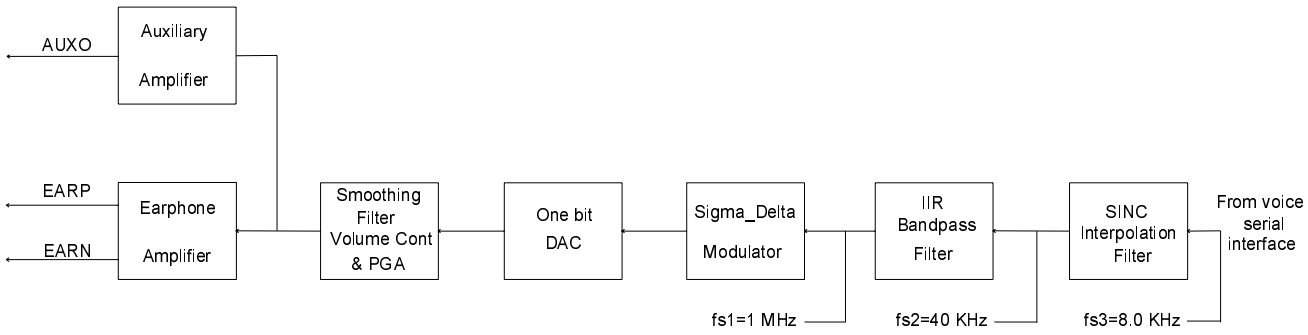

Figure:7 Voice DAC block diagram 600-0807

8.2.6 Auxiliary A/D

VEGA provides 5 A/D inputs.

G520 takes advantage of the A/D inputs on VEGA allowing external power to be monitored with just 2 resistors each and no need for a buffer transistor.

VEGA input	Pin Number	Use	Range
ADC0	36	Battery Voltage	0 = 0V 3FFh = 9.0V
ADC1	37	Battery Type	0~136h = Ni-MH 137~3FFh = Li-ION
ADC2	38	Battery Temperature	0D5h = +70°C 249h = +25°C 3FBh = -20°C
ADC3	39	nADP _SENSE	0~168h = Data Adaptor 17C~1EDh = RS232 Direct Cable 230~2C0h = SMS Cable 2L8~365h = Headset Adaptor Other value = No Adaptor
ADC4	40	Current	0h = 0 mAh 3FFh = 800 mAh

9 POWER SUPPLIES

9.1 Introduction

This section describes the Power Supply Unit (PSU) used on the G520 logic PCB and the method by which it is controlled.

This section has detailed information on:

1. An overview of the circuit functionality.
2. Powering-up the phone.
3. Powering-down the phone.
4. Power management.

9.2 Overview

The circuit contains two linear regulators; 3.6 V for the LCD and 3.0 V for everything else, analogue and digital. There is a low current step-up converter to provide 5.0 V for the SIM interface. The battery voltage detector, nominally set to 3.6 V prevents the phone from powering up if the battery voltage is very low (to avoid deep battery discharge) and also provides an interrupt to shut down the phone if the battery is suddenly removed, primarily to protect the SIM.

The SIM power supply should be enabled and disabled as part of the SIM interface procedures and therefore falls outside the scope of this document

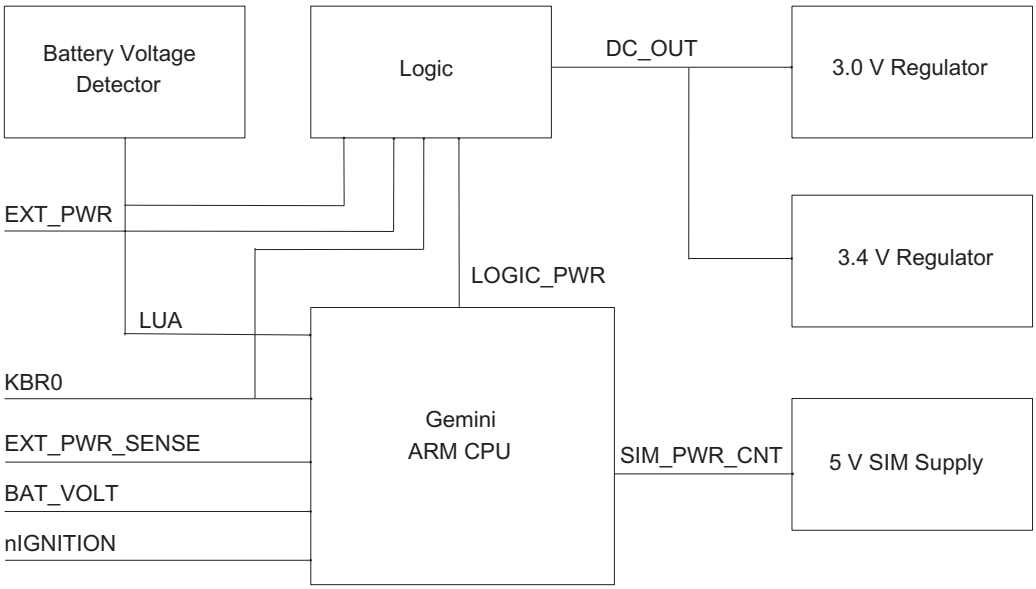

Figure:1 Block diagram 520-0901

Signal	CPU I/O	Description
KBR0	I	Power key. This signal is connected to the KBR0 pin on GEMINI. When the power key is held down this signal is HIGH.
EXT_PWR	NC	External power supply from AC adapter etc. When present the PSU is forced on.
EXT_PWR_SENSE	I	EXT_PWR scaled and sensed by the CPU as an analogue voltage.
BAT_VOLT	I	Scaled battery voltage. This parameter is measured by the CPU and used for gas gauging, regulating LED brightness, charging and to decide when to power-down etc.
LUA	I	External interrupt to the CPU. The voltage detector output goes LOW when the battery voltage drops below 3.6 V. If the phone is on, this signal forces the PSU off and the interrupt initiates an emergency power-down procedure. If the phone is off, a LOW on this signal will lock the PSU off. EXTINT can override all signals except EXT_PWR.
LOGIC_PWR	O	Signal generated by the CPU to hold the PSU on. Active high.
DC_OUT	NC	Chip select to the 3.0 and 3.4 V regulators. Active low.
SIM_PWR_CNT	O	Output from the CPU to enable the SIM 5.0 V supply. Active high.
NIGNITION	I	Vehicle ignition. When the vehicle ignition is on, this signal is LOW. This is sensed by the CPU as an analogue voltage.

9.3 Power-up

The power-up procedure has two phases. If an initial check to see if the battery is in good condition is successful, the second phase determines the source of the power-up request, key press, external power, accessory, etc. and acts accordingly.

The phone can be defined as powered-on whenever the linear regulators are active. It is not always obvious to the user that the phone is powered-on as it may be in one of four modes:

Mode	Description
Sleep	In this mode the CPU has been prevented from deactivating the linear regulators by EXT_PWR. There is no CPU activity.
Charge	The CPU is alive but may perform *only* battery charging functions and monitor the power key.
Restricted	LEDs light, beeps, can charge battery etc. but it is *not* permitted to use the radio.
Active	The mobile is fully functional; LEDs light, beeps, search for network etc.

9.3.1 Battery Condition

The CPU must check the battery condition before deciding to power-up. The CPU can measure battery voltage and temperature. If the temperature measurement is invalid, giving a ridiculous temperature reading, a non-standard battery has been fitted, the battery is missing or the whole phone is operating far outside its specified temperature range. In any of these cases the phone must not power-up. The CPU will regularly monitor the battery condition while the phone is on.

If EXT_PWR is present the regulators will be forced on and the CPU will not be able to deactivate them. If the CPU wants to power-down, all it can do is to enter sleep mode.

Battery Voltage (V)	Temp. reading	EXT_PWR_SENSE	Result
X (don't care)	invalid	0.5 V	Power-down (battery fault)
X	invalid	1.2 V	Sleep (battery fault)
<4.0	X	<0.5 V	Power-down (low battery)
<4.0	valid	1.2 V	LOW
>4.0	valid	X	OK

9.3.2 Power-up Sequence

The power-up sequence can be initiated by pressing the power key or by the presence of an external power source on the signal EXT_PWR. Both enable the linear regulators and the CPU becomes active. The CPU must then check the battery condition; if the phone is not required to power-down or sleep immediately, the result must be OK or LOW. The CPU then checks to see if a hands-free unit is connected by polling the nHF_SENSE signal, LOW when HF is connected.

Now the CPU can make the decision whether to remain powered-up or not according to the truth-table below. In each case the active parameters are shaded.

Battery Condition	HF	EXT_PWR_SENSE	nIGNITION	KBR0	LOGIC_PWR	Mode
OK	X	X	X	1	1	active
LOW	X	>1.2 V	X	1	1	restricted
OK or LOW	no	>1.2 V	X	0	1	charge
OK	yes	>1.2 V	<0.5 V	0	1	active or charge
LOW	yes	>1.2 V	<0.5 V	0	1	restricted or charge

With a hands-free, the phone can be configured via the MMI to power-up and down with transitions of the vehicle ignition. These are sensed by the CPU on nIGNITION, LOW when the ignition is on.

Any other state than those in the table will cause the phone to deactivate the PSU by setting STAY_ALIVE LOW.

While the CPU is active, it must monitor the battery condition and accessory connectivity and change state accordingly.

Current Mode	HF	EXT_PWR_SENSE	nIGNITION	KBR0	Battery Condition	New Mode
Charge	X	X	X	1	OK	active
Charge	X	1.2 V	X	1	LOW	restricted
Restricted	X	X	X	0	OK	active

9.4 Power-down

There are two power-down procedures:

Procedure	Description
Normal power-down	In this case, the software has full control over the power-down procedure. Calls can be terminated gracefully etc. In some cases the PSU is not deactivated but there is a change of operating mode.
Emergency power-down	This situation is caused by battery removal and is flagged by EXTINT. In this case the CPU only has time to perform a subset of the normal procedure. The priority is to prevent corruption of SIM data.

The truth-table for the power state transitions are shown below, the cause of a transition is shaded. In some cases the phone does not power-down completely but may enter a state of reduced functionality, e.g. from active to charge mode.

When the new mode is OFF or sleep, the CPU will set STAY_ALIVE LOW.

Current mode	Battery Voltage	HF	Nignition	EXTINT	KBR0	EXT_PWR_SENSE	power-down	New mode
X		X	X	1	X	<0.5 V	normal	OFF
X	X	X	X	0	X	X	emergency	OFF
X	X	X	X	1	1	<0.5 V	normal	OFF
active	<4.0 V	X	X	1	0	>1.2 V	normal	restricted
active	<4.0 V	no	X	1	1	>1.2 V	normal	charge
active	<4.0 V	yes	>2.5 V	1	1	X	normal	OFF
active	<4.0 V	yes	<0.5 V	1	1	>1.2 V	normal	charge
active	<4.0 V	yes	>2.5 V	1	0	X	normal	OFF
active	X	no	X	1	1	>1.2 V	normal	charge
active	X	yes	<0.5 V	1	1	>1.2 V	normal	charge
active	X	yes	>2.5 V	1	1	X	normal	OFF
active	X	yes	>2.5 V	1	0	>1.2 V	normal	OFF
active	X	X	X	1	0	<0.5 V	normal	OFF

9.5 Power Management

The power supply circuit supplies regulated power to the base-band parts, controls battery charging and monitors battery usage.

G520 must achieve two types of battery operation - 4 cell Ni-MH and 2 cell Li-ION.

The power supply section consists of four parts;

1. Power-on circuitry.
2. Voltage regulators.
3. Battery charging circuitry.
4. Power fail detection.

To reduce the cost of the phone four Ni-MH cells are used as the standard power source. The Li-ION standard battery gives 400 mAh (typical) capacity. The optional Ni-MH battery gives 670 mAh capacity.

Battery operating voltage range:

4.5 V	(minimum safe discharge)
6 V	(maximum fully charged Ni-MH)
8.2 V	(maximum fully charged Li-ION)

The G520 battery management operates with the following voltage levels:

Battery Voltage	Ni-MH	
B-Icon 3 bar	4.90<	
B-Icon 2 bar	4.75<	<4.90
B-Icon 1 bar	4.50<	<4.75
LVA		<4.50

NOTE:

During charging, the voltage could rise as high as 9.4 V; all circuitry connected to the battery must be designed to operate up to this voltage.

A block diagram for a four cell power supply is shown in Figure 2 below. Note that the battery voltage is stepped-up to power 5 V SIM cards or the 5 V RF power amplifier. This circuit also shows a Power-On-Reset (POR) to hold the CPU in a reset state while the supply voltage and system clock stabilise.

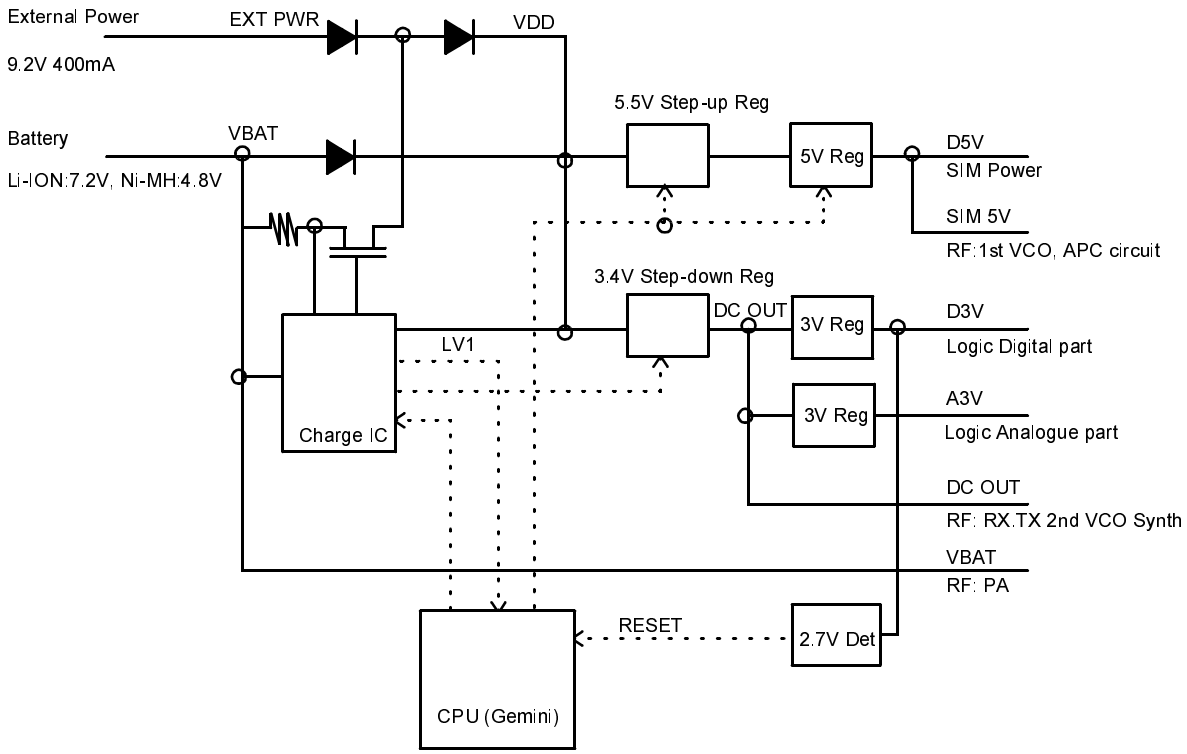

Figure:2 Power supply block diagram 600-1002

9.5.1 Power On Circuit

There are two mechanisms for powering on the Hand-held, Power Key or External power. The Hand-held is kept powered on by the CPU, stay alive, or external power. This means that the phone remains powered-up all the time that external power is present. To minimise drain on external power, for example while the phone is connected to a car kit with ignition off, the phone is put into sleep-mode to give an average power use of less than 2 mA. For a 20 Ah car battery the phone could be left connected and powered off for approximately 416 days before the battery would run flat, assuming no battery self discharge.

Voltage Regulation

Using four cell Ni-MH or two cell Li-ION with 3.0 V logic gives no problems with high regulator voltage dropout. Especially in Li-ION cells, high voltage dropout reduces the efficiency more than a small voltage dropout. To increase the current consumption efficiency, the G520 uses 3.4 V step-down DC/DC voltage regulators. The DC/DC step-down circuitry uses two regulators on the LOGIC side and three regulators on the RF side to reduce the power loss to a minimum.

The G520 has the following power sources:

D3V : Baseband power supply for digital circuitry (GEMINI and Memory)

Voltage	3.0 V ± 5 %
Current	200 mA max.

A3V : Baseband power supply for Analogue circuitry (VEGA and Voice-Memo)

Voltage	3.0 V ± 5 %
Current	200 mA max.

D5V, SIM5V : SIM power supply (SIM access interface)

Voltage	5.0 V ± 5 %
Current	50 mA max.

VDD : Common power supply

Voltage	8.5 V max.
Current	200 mA max.

VDD power source is supplied by either the battery or the EXT_PWR. VDD supplies the 3.4 V step-down DC/DC converter, 5.5 V step-up DC/DC converter and the LEDs.

DCOUT : Step-down DC/DC converter output (input power for D3V and A3V regulators)

Voltage	3.445 V ± 5 %
Current	250 mA max.

Ext_PWR : External power supply

Voltage	9.2 V ± 0.2 V
Current	430 mA ± 30 mA

VBAT : Battery power supply

	Ni-MH	Li-ION
Voltage	4.8 V nominal	7.2 V nominal

9.5.2 Battery Charging Circuit

The CPU within the phone controls the battery charging. When external power is present the phone is automatically switched on. If rechargeable cells are detected and the temperature is within specified limits the charger starts using a rapid charge algorithm.

With Ni-MH cells, charging is determined by delta V, with time, temperature and voltage safeguards. With Li-ION, cells, charging is determined by constant current, with time, temperature and voltage safeguards.

Deeply Discharged Batteries

When a battery is deeply discharged, there may not be enough power to power on the phone for charging. In this case the charging circuit must automatically detect if the batteries are rechargeable and start slow trickle charge until there is enough power to switch on the phone.

9.5.3 Power Fail

The SIM card contains EEPROM; if power fails while the SIM is active, the SIM memory may be corrupted as the voltage drops out of specification.

The nVLA_INT is a non-maskable interrupt to the CPU which forces exception processing whenever the battery voltage drops below 3.2 V.

NRESET signal is connected to the GEMINI reset terminal. The nRESET signal is generated by a 2.7 V voltage detector.

10 ACCESSORIES

10.1Handsfree Unit - Circuit Description

10.1.1 General Description

The handsfree unit consists of audio processing, power supply and external power for the charging circuitry within the handheld unit.

A digital signal processor (DSP) is used to remove the local echo or feedback created between the loudspeaker and microphone.

The analogue speech signal is converted into digital form using CODECs, which perform analogue to digital and digital to analogue conversion on the received and transmitted audio.

The handheld unit has an internal charging circuit. The handsfree unit uses this facility to charge the attached battery.

The connector at the base of the handheld unit contains a mechanical RF switch. When the connector is in use the RF signal is disconnected from the internal antenna and sent out through the handsfree unit RF cable.

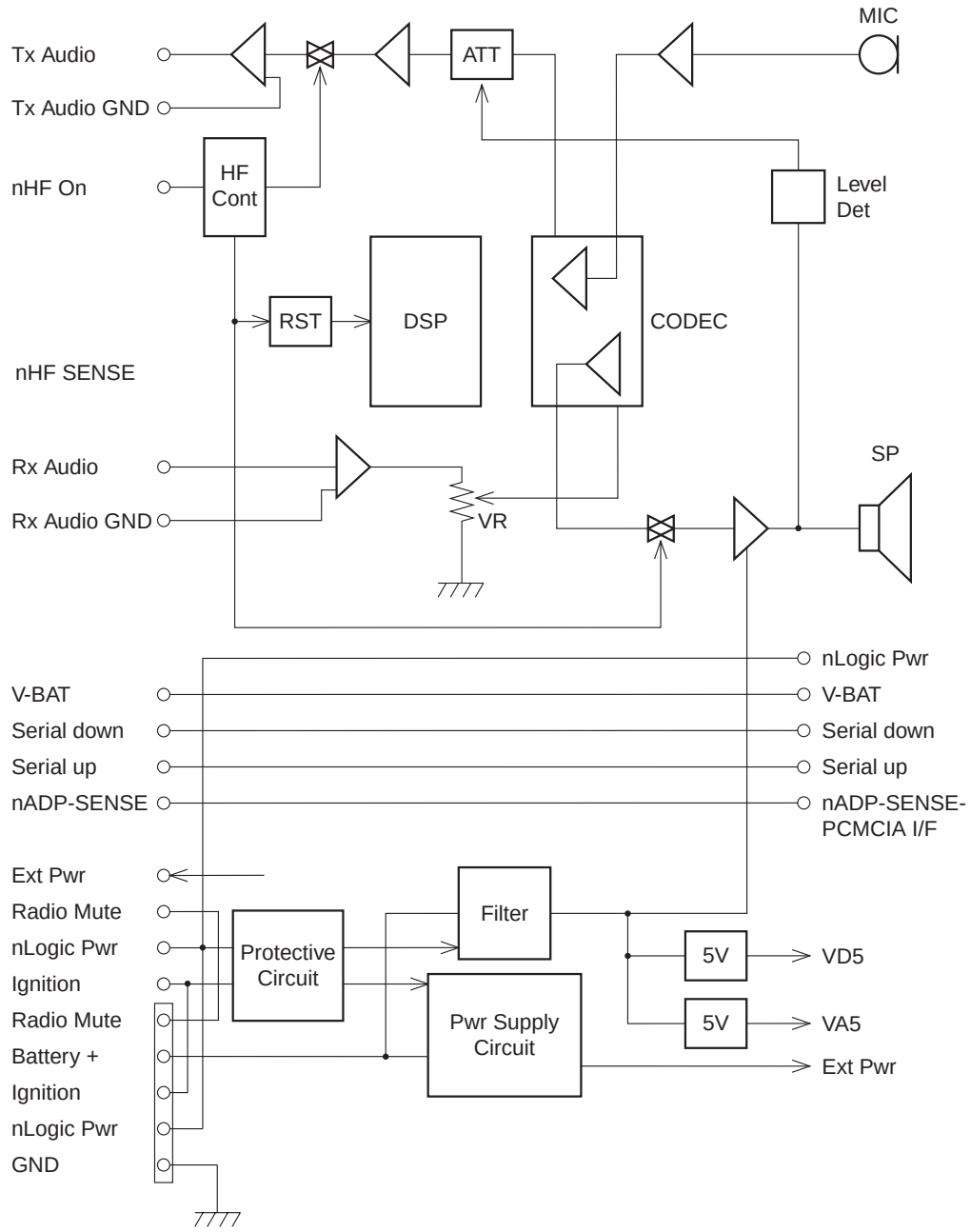

Figure:1 G520 Hands Free Block diagram 520-1001

10.1.2 Detailed Description

TX Audio

The external microphone connects to J301. The voice signal from the microphone is amplified by U301 and converted into a digital form by U304, a CODEC containing an analogue to digital converter for the transmitted audio, and a digital to analogue converter for the received audio.

The digitised speech is processed by U306 (DSP echo canceller). The output from pin 13 of the DSP is reconverted into analogue form by U304 (CODEC). Further amplification is provided by U301 and U315. The audio signal is then transmitted via P201 to the handheld unit for further processing.

RX Audio

The voice signal from the handheld unit is amplified by the handsfree unit. P201 connects the audio signal from the handheld to the handsfree unit via pin 4. U301 provides initial amplification of the received audio. R324 is a variable resistor controlled by the thumbwheel on the side of the handsfree case, providing volume level control.

The voice signal is converted into digital by U304 and processed by the DSP (U306). U304 reconverts the speech into analogue form. Further amplification is provided by U308, the output of which passes to the internal speaker via P300. If an external speaker is connected to P300 then the path to the internal speaker is broken and the audio is transmitted to the external source.

Power Supply

Supply for the handsfree unit is provided via J201. Reverse voltage protection is provided by D201. An active low signal from the handheld unit (nLogic Pwr) switches Q202 and Q203 ON. Activation of Q203 switches the base of Q205 low, enabling the positive supply through Q205 to the voltage regulators. D202 provides over-voltage protection. Should the supply exceed 16 V, D202 will break down switching Q201 ON and sending the base of Q203 low, switching Q205 OFF.

The output from Q204 takes two paths. The positive 13 V supply is regulated down to 5 V by U302 and U303. U302 supplies the DSP, CODECs and reset control. U303 supplies the audio amplifiers.

The 13 V supply is also regulated down to 6.7 V for the external power supply for the handheld unit. U101 is a switching regulator that provides this function.

Level Detector

A sample of the output audio is taken from P300. U309 detects the audio signal level on pin 1. If the detected speaker audio level is high, then pin 6 will go low. A low signal on pin 6 switches Q305 ON, switching positive supply onto Q306. Q306 switches R305 into the TX audio path, reducing the audio level.

10.1.3 Test Points

TP No.	DESCRIPTION	BOARD LOCATION
TP101	Switching Voltage Regulator	U102 Pin 2
TP201	External power	P201 Pin 15
TP202	nLogic Power	P201 Pin 14
TP203	Battery + (car)	P203 Pin 1
TP300	TX Audio (To the handheld unit)	P201 Pin 3
TP301	Output Amplifier Power	Q205 Pin E
TP302	GND	U308 Pin 3
TP304	RX Audio (To the handheld unit)	P201 Pin 4
TP305	Audio GND	P201 Pin 5
TP306	nHF on	P201 Pin 7
TP307	Mic override speaker	R355, R309
TP309	Audio GND	P301 Pin 2
TP310	Mic	P301 Pin 1
TP311	Speaker	J300 Pin 2
TP312	Audio GND	J300 Pin 1
TP313	U306 pin 3 HCL	U306 Pin 3

10.1.4 Adjustment and Calibration

The adjustments that can be made on the handsfree unit are to the external power supply. These are made by adjusting two variable resistors on the PCB. The procedure must be followed if the switching voltage regulator or any other part of the external power supply is replaced.

10.1.5 Procedure

1. Connect up the Handsfree unit as for normal testing, but do not connect the Handheld unit.
2. Measure the external voltage power supply.
3. Adjust R102 so that this voltage is 7.8 V ± 0.07 V.
4. Once the handheld unit is connected and in a call use R144 to adjust the maximum current supplied.

10.2Dual Charger

10.2.1 Circuit Description

A battery present is detected by the TH input, and battery type is detected by the S input. The S input is open-circuit on a small battery, pulling the base of Q13 high, turning it off. The base of Q2 is pulled low through R24, turning Q2 ON. This switches the extra control resistor VR1 into circuit, increasing the timer clock rate. VR2 is used to control the clock rate when a large battery is connected.

The charging circuit is controlled by the current drawn by the handheld unit. If the handheld unit receives a call and thus requires greater than 300 mA, then it switches the charger off, only switching it back on again when the current drops below 200 mA. These current levels are controlled by VR3 (set the stop point) and VR4 (set the start point).

The power out for the handheld unit is protected by Q11, Q16, and Q5. When the power is connected, a small current can flow through R27 and the bleed resistor R33. Through the potential divider R39 and R38, this turns Q5 ON, turning Q16 ON. Should the output CN2 become accidentally short-circuited the base of Q5 becomes low turning Q5 OFF. This pulls the base of Q16 high, turning Q16 OFF and shutting off the power.

10.2.2 Adjustment Procedure

If any of the main components in the charger are replaced then the following procedure must be followed. The procedure first adjusts the charge rate timer for each battery, followed by the control current levels for switching the charger on and off.

Connect the charger as shown in the following diagram.

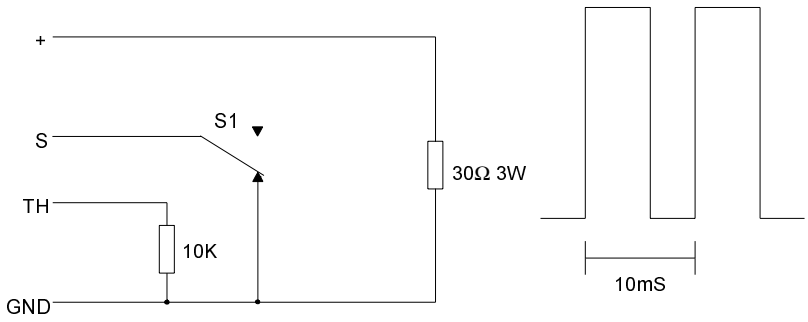

Figure:2 Charger Connections 600-1101

1. Adjust VR2 until the pulses on pin 3 of IC 2 have a period of 10 ms ± 0.5 ms. Open the switch S1 and adjust VR1 until the pulses have a period of 3.45 ms ± 1.5 ms.
2. With S1 closed connect a load of 300 mA ± 5 mA across the output that goes to the handheld unit.
3. Adjust VR3 so that clock pulses on pin 3 of IC 2 stop, i.e. there is a steady level of 5 V or 0 V.
4. Reduce the load to 200 mA ± 5 mA and adjust VR4 so that the pulses start again.

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